## Junction Field Effect Transistor (JFET)

The single channel **junction field-effect transistor (JFET)** is probably the simplest transistor available. As shown in the schematics below (Figure 6.13 in your text) for the n-channel JFET (left) and the p-channel JFET (right), these devices are simply an area of doped silicon with two diffusions of the opposite doping. Please be aware that the schematics presented are for illustrative purposes only and are simplified versions of the actual device. Note that the material that serves as the foundation of the device defines the channel type.
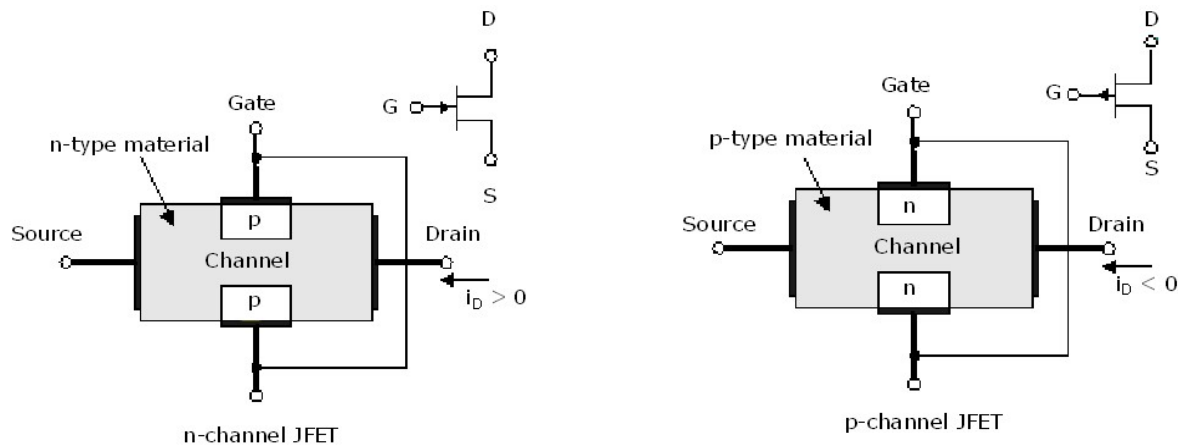
Like the BJT, the JFET is a three terminal device. Although there are physically two gate diffusions, they are tied together and act as a single **gate** terminal. The other two contacts, the **drain** and **source**, are placed at either end of the channel region. The JFET is a symmetric device (the source and drain may be interchanged), however it is useful in circuit design to designate the terminals as shown in the circuit symbols above.

The operation of the JFET is based on controlling the bias on the pn junction between gate and channel (note that a single pn junction is discussed since the two gate contacts are tied together in parallel – what happens at one gate-channel pn junction is happening on the other). If a voltage is applied between the drain and source, current will flow (the conventional direction for current flow is from the terminal designated to be the gate to that which is designated as the source). The device is therefore in a normally on state. To turn it off, we must apply an appropriate voltage to the gate and use the depletion region created at the junction to control the channel width.

The following discussion is going to focus on the n-channel JFET (analogous to the npn BJT). The operating and characteristics of the p-channel JFET may then be deduced by making the necessary changes to voltage polarities and

current directions. The following definitions and conditions will hold throughout our analysis:

➢ The source of the JFET will provide a common ground for all device terminals. While this is not required, it is common practice.
➢ The voltage applied to the drain will be designated v_{DD}. Note that in some other texts and literature this is referred to as v_{DS}.
➢ The voltage applied to the gate will be designated v_{GG}. Note that in some other texts and literature this is referred to as v_{GS}.

The n-channel JFET connected to the voltages sources v_{DD} and v_{GG} is presented to the right (Figure 6.14a of your text). The polarity indicated for v_{DD} means that the electrons in the channel will be attracted to the drain and conventional current will flow in the direction indicated by i_D (remember that negative charges moving in a negative direction have the same effect as positive charges moving in a positive direction). The polarity voltage applied to the gate (v_{GG}) ensures that the gate-channel pn junction will be reverse biased and essentially no current will flow (the reverse bias saturation current is considered negligible). The JFET is a voltage-controlled device, with two controlling voltages (v_{DD} and v_{GG}). We are going to look at these individually and then combine the results for the overall JFET characteristics.
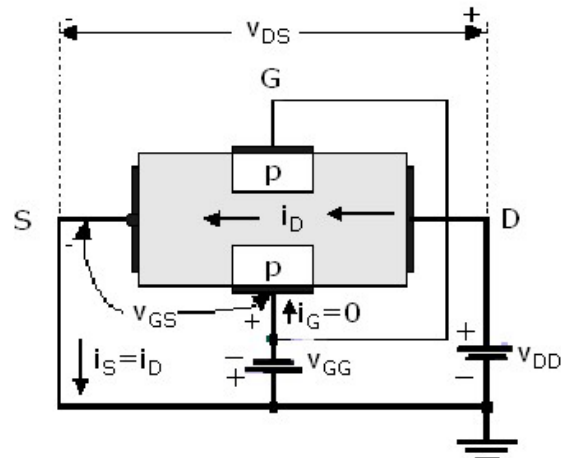
JFET Drain-To-Source Voltage Variation

To follow the development in your text, the first effect we're going to look at is the variation of the drain-to-source voltage through the applied voltage v_{DD}. The figure to the right is a modified version of Figure 6.14b in your text. For purposes of this discussion, the gate-to-source voltage is zero, although the same will hold true for any
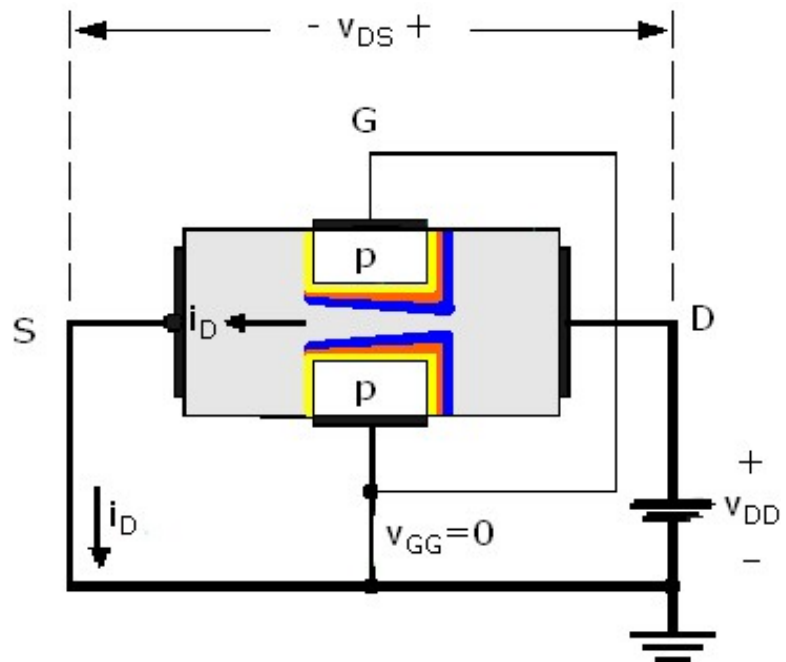
suitable v_{GG} (hang on, that part is coming up next).
Anyway, please bear with my attempt at artwork as we go through this!

For a constant v_{GG}, the effect of v_{DD} variation may be illustrated as follows:

➢ v_{DD} must be greater than zero for current to flow in the direction defined in an n-channel JFET. The applied v_{DD}, or the voltage between drain and source (ground) appears as a voltage drop across the length of the channel, with the voltage increasing along the channel from source to drain (i.e., $v_{DS}=0$ at the source, $v_{DS}=v_{DD}$ at the drain). We're also going to assume a constant doping so that the voltage variation in the channel is linear (v_{GG} also affects this – talked about below).
➢ When v_{DD} is very small, the voltage variation in the channel is very small and it has no effect on the channel shape. For this case, the depletion region is only due to the pn junction as shown in yellow in the figure.
➢ As v_{DD} increases, the increasing potential at the drain reverse biases the pn junctions. Since the voltage drop across the channel increases from source to drain, the reverse bias of the pn junction also increases from source to drain. Since the depletion region is a function of bias, the depletion region also gets wider from source to drain, causing the channel to become tapered as shown in red in the figure. The current still increases with increasing v_{DD}, however there is no longer a linear relationship between v_{DD} and i_D since the channel resistance is a function of its width.
➢ Further increases in v_{DD}, for example, blue in the figure, result in a more tapered shape to the channel and increasing nonlinearities in the i_D-v_{DD} relationship.
➢ This process continues until a v_{DS} is reached where the depletion regions from the pn junctions merge. Analytically, this occurs when the gate-to-drain voltage v_{GD} is less than some threshold V_P (note that some sources denote the threshold as V_T) and is known as the **pinch-off point**. At this point, the drain current saturates and further increases in v_{DS} result in little (ideally zero) change in i_D. For the case $v_{GG}=v_{GS}=0$, the drain current at pinch-off is called the **drain-source saturation current, I_{DSS}**. Operation beyond the pinch-off point ($v_{DS} > v_{GS} - V_P$ for an n-channel device) defines the **normal operating** or **saturation region** of the JFET.

JFET Gate-To-Source Voltage Variation

For a constant v_{GG}, varying v_{DS} yields a single i_D-v_{DS} characteristic curve. To develop a family of characteristic curves for the JFET device, we need to look at the effect of v_{GS} variation. The figure to the right is a simple illustration of the variation of v_{GG} with a constant (and small) v_{DD}. Recall from the previous discussion that, if v_{DD} is small, v_{DS} is small and the channel width is essentially constant. In the figure, the increasing width of the pn junction depletion region (illustrated from yellow to red to blue), is due to the increasing reverse bias of the junction resulting from the application of a negative v_{GG} of increasing magnitude. As the depletion widths increase, the channel width decreases, resulting in a lower conductivity (higher resistivity) of the channel. As v_{GS} is made more negative (for an n-channel device), a value of v_{GS} is reached for which the channel is completely depleted (no free carriers) and no current will flow regardless of the applied v_{DS}. This is called the **threshold**, or **pinch-off**, **voltage** and occurs at $v_{GS}=V_{GS(OFF)}$. The threshold voltage for an n-channel JFET is negative ($V_P < 0$, using your text's notation).
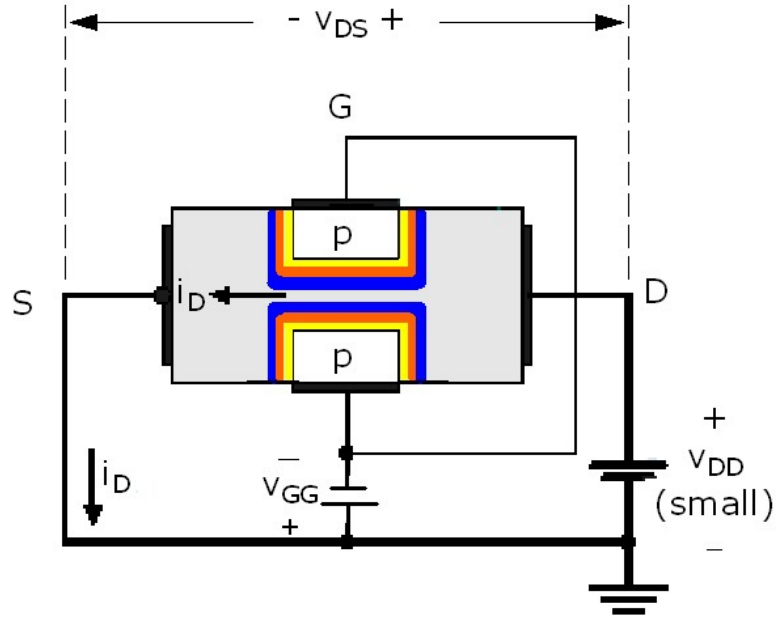
If we now apply the v_{DS} variation effect, we can see that pinch-off will occur for lower values of v_{DS} since we have less of a channel to start with (resulting in lower values of i_D at pinch-off). By combining the effect of v_{DS} and v_{GS} variations, a family of characteristic curves similar to the figure at the right (based on Figure 6.16a of your text) will be generated for the n-channel JFET.
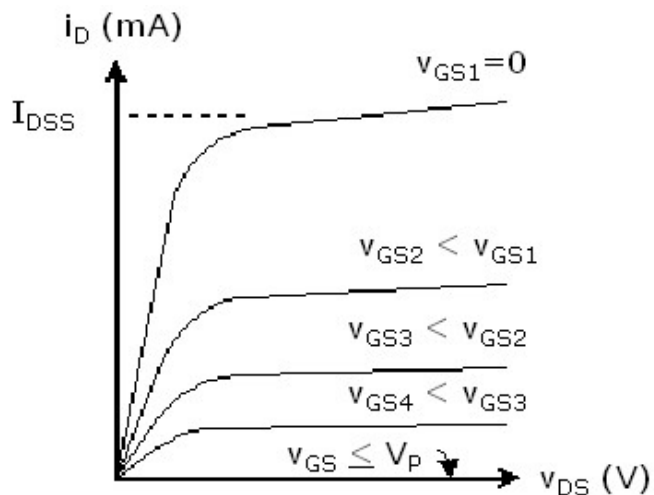
Similar results are illustrated in the family of characteristic curves presented to the right, and may be obtained for a p-channel JFET by following the previous discussion with the following modifications:

- The polarity of v_{DS} is switched since the majority carriers are holes.
- The current flows out of the drain terminal, yielding a negative current with respect to conventional current direction (drain to source was defined as the positive direction).
- The threshold voltage of a p-channel JFET is positive and the channel is depleted when $v_{GS} \geq V_P$.
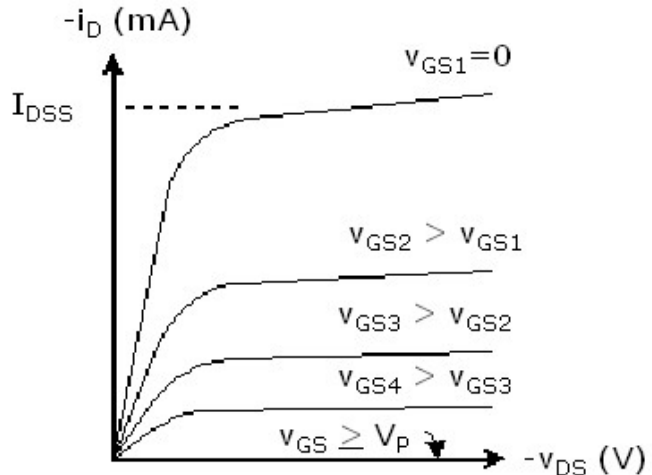
JFET Transfer Characteristics

The **transfer characteristic** for a FET device is presented as a plot curves representing drain current as a function of drain-to-source voltage for a sequence of constant gate-to-source voltages, as illustrated in the figures above for the n-channel and p-channel JFET. After the JFET reaches saturation, i_D remains relatively constant with a very small slope for further increases in v_{DS} (the slope of the curves would be zero for an ideal device).

A complete transfer characteristic for an n-channel device is shown in Figure 6.17 in your text and is presented (slightly modified) to the right.
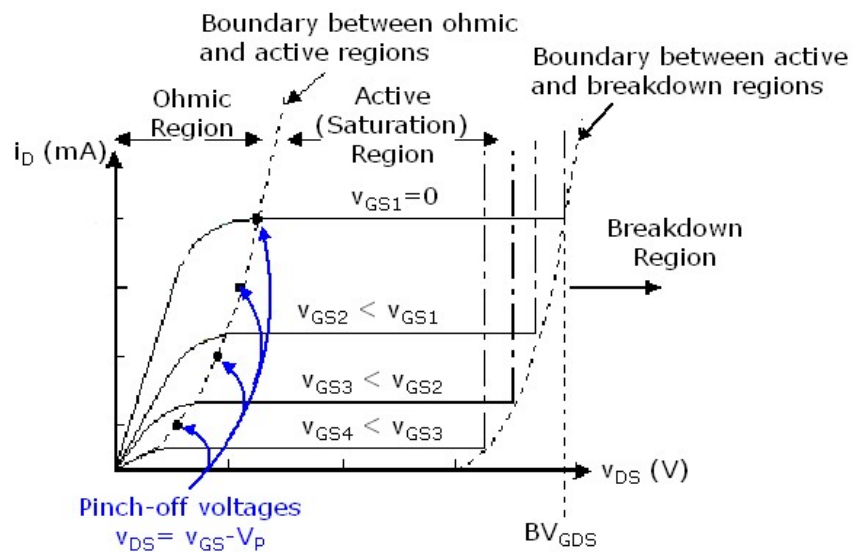
Below pinch-off, the channel essentially behaves like a constant resistance as we discussed earlier. This linear region of operation is called **ohmic** (or sometimes triode), and is where the JFET may be used as a resistor whose value is determined by the value of v_{GS}. The

transistor may function as a variable resistor when operated in the ohmic region by varying the value of v_{GS}. However, note that as the magnitude of v_{GS} increases, the range of v_{DS} where the transistor may be operated as an ohmic resistor decreases. In the ohmic region, the potentials at all three terminals strongly affect the drain current, and the drain current obeys the relationship:

$$i_D = K\left[2(v_{GS} - V_P)v_{DS} - v_{DS}^2\right], \text{ where } K = \frac{I_{DSS}}{V_P^2}$$ (Equations 6.39 & 6.40)

Beyond the knee of the ohmic region, the curves become essentially flat in the **active** (or **saturation**) **region** of operation. This is where we want to be to perform linear amplification! To **operate in the linear region**, it is standard practice to **define the dc bias current at the Q-point as between 30% and 70% of I$_{DSS}$.** This locates the Q-point in the most linear region of the characteristic curves. **To locate the Q-point near the center of the linear operating region,** your author suggests using **I$_{DQ}$=I$_{DSS}$/2 and V$_{GSQ}$=0.3V$_P$.**

The drain current in the saturation region may be defined by using the Shockley equation (Equation 6.16 in your text) in terms of the drain-source saturation current (I$_{DSS}$), the threshold voltage (denoted V$_P$ in your text) and the applied gate-to-source voltage (v$_{GS}$) as:

$$i_D \cong I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2.$$ (Equation 6.19)

The parameters I$_{DSS}$ and V$_P$ (sometimes called V$_T$ or V$_{GS(OFF)}$ on the data sheets) are generally given by the manufacturer. *This makes things a little easier than for the MOSFETs, where a conductance parameter is given and you have to calculate your own I$_{DSS}$ value! Just a little preview of coming attractions...* However, be aware that I$_{DSS}$ is a function of temperature and both I$_{DSS}$ and V$_P$ are strongly functions of the manufacturing process. It is therefore very important that the manufacturer's data sheets be consulted to ensure that operational conditions and desired results are within spec.

To account for the finite slope of the curves in the active region, the effect of a device parameter (λ), known as the **channel length modulation parameter**, that is analogous to the inverse of the BJT Early voltage (V_A^{-1}) is included in the expression for the drain current.
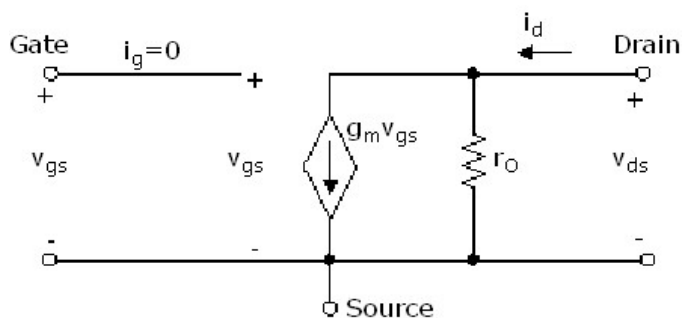
$$i_D \cong I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS})$$

(Equation 6.20)

Usually, especially for large-signal analysis or biasing, λ is small enough that $|\lambda v_{DS}| \ll 1$ and the expression of Equation 6.19 is sufficient.

As v_{DS} continues to increase, a point is reached when the drain-to-source voltage becomes so large that **avalanche breakdown** occurs at the drain end of the gate-channel junction. At the breakdown points, shown by dashed lines in the figure, i_D increases sharply with negligible increases in v_{DS}. The value of v_{DS} denoted BV_{GDS} is the breakdown voltage of the pn junction (i.e., when $v_{GS}=0$). As can be seen in the figure above, the breakdown voltage is also a function of v_{GS} – as the magnitude of v_{GS} increases (more negative for n-channel and more positive for p-channel) the breakdown voltage decreases.

JFET Small-Signal Model

The ac small-signal model of the JFET is given in Figure 6.18 of your text and is reproduced to the right. Expressions for the transconductance g_m and the output resistance r_O may be derived from Equation 6.20 as follows:

$$g_m = \frac{\partial i_d}{\partial v_{gs}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)(1 + \lambda v_{DS})$$

$$r_O = \frac{\partial v_{ds}}{\partial i_d} = \frac{1}{I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \lambda}$$

(Equation 6.22)

where

➢ ac quantities are denoted by lower case variables and lower case subscripts (remember the rules?)
➢ Total instantaneous quantities (ac+dc) are denoted by lower case variables and upper case subscripts.
➢ dc quantities are denoted by upper case variables and upper case subscripts. Note that V_{GS} is considered a dc quantity since we are operating on a single curve where v_{GS} is constant.

➢ We will see in the next section that, except for a few notation changes, this is exactly what we come up with for the MOSFET!

The MOSFET (that we're going to talk about next) has a number of advantages over the JFET. Notably, the input resistance of the MOSFET is higher than that of the JFET (remember that an ideal input resistance is infinity). This characteristic, in addition to the many other advantages of the MOSFET, has made MOS the predominant FET technology today. Nonetheless, the JFET is still used in limited situations, especially for analog applications.

Finally, we're going to end this section with a summary of JFET characteristics:

	n-channel	p-channel
V_P	< 0	> 0
Normally	On	On
To turn device off	$v_{GS} \leq V_P$	$v_{GS} \geq V_P$
K	$\dfrac{I_{DSS}}{V_P^2}$	
$\lambda\ (= V_A^{-1})$	> 0	< 0
To operate in ohmic region	$v_{DS} < v_{GS} - V_P$	$v_{DS} > v_{GS} - V_P$
Drain current in ohmic region	$i_D = K\left[2(v_{GS} - V_P)v_{DS} - v_{DS}^2\right]$	
To operate in saturation region	$v_{DS} \geq v_{GS} - V_P$	$v_{DS} \leq v_{GS} - V_P$
	$\|v_{DS}\| < \|V_{breakdown}\|$	
Drain current in saturation region	$i_D \cong I_{DSS}\left(1 - \dfrac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS})$	
Output resistance	$r_O = \dfrac{1}{I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 \lambda}$	
Transconductance	$g_m = -\dfrac{2I_{DSS}}{V_P}\left(1 - \dfrac{V_{GS}}{V_P}\right)(1 + \lambda v_{DS})$	