MULTICHIP PACKAGING

Multichip Modules

- A single unit (package) containing two or more chips and an interconnection substrate which function together as a system building block.

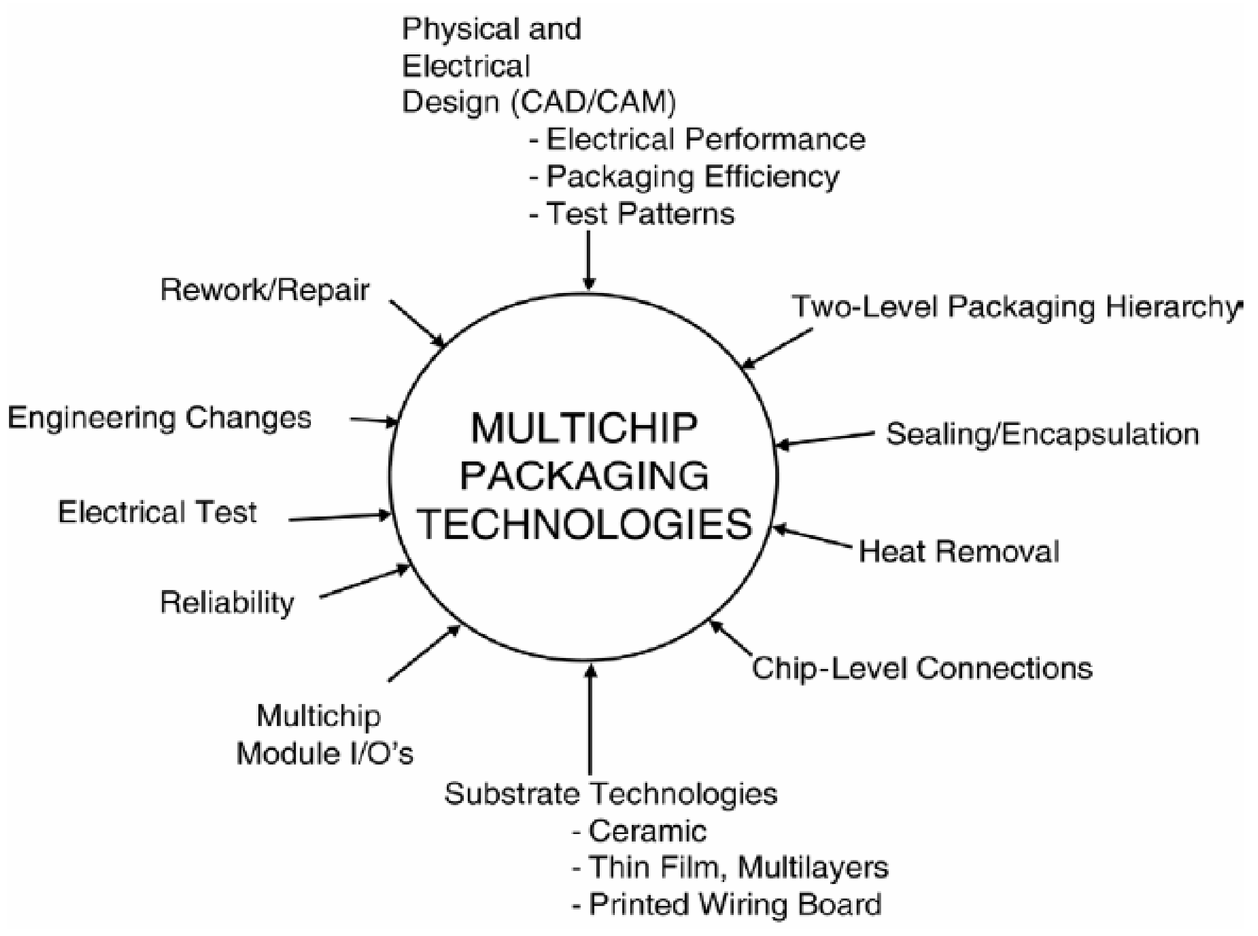
- Classification Requirements

  $A_c \geq 0.5\ A_s$

  Where A_c is the area of the semiconductor or chip.

  A_s is the area of the substrate (package or carrier)

Multichip Modules at the System Level



Multichip Modules

- Functions

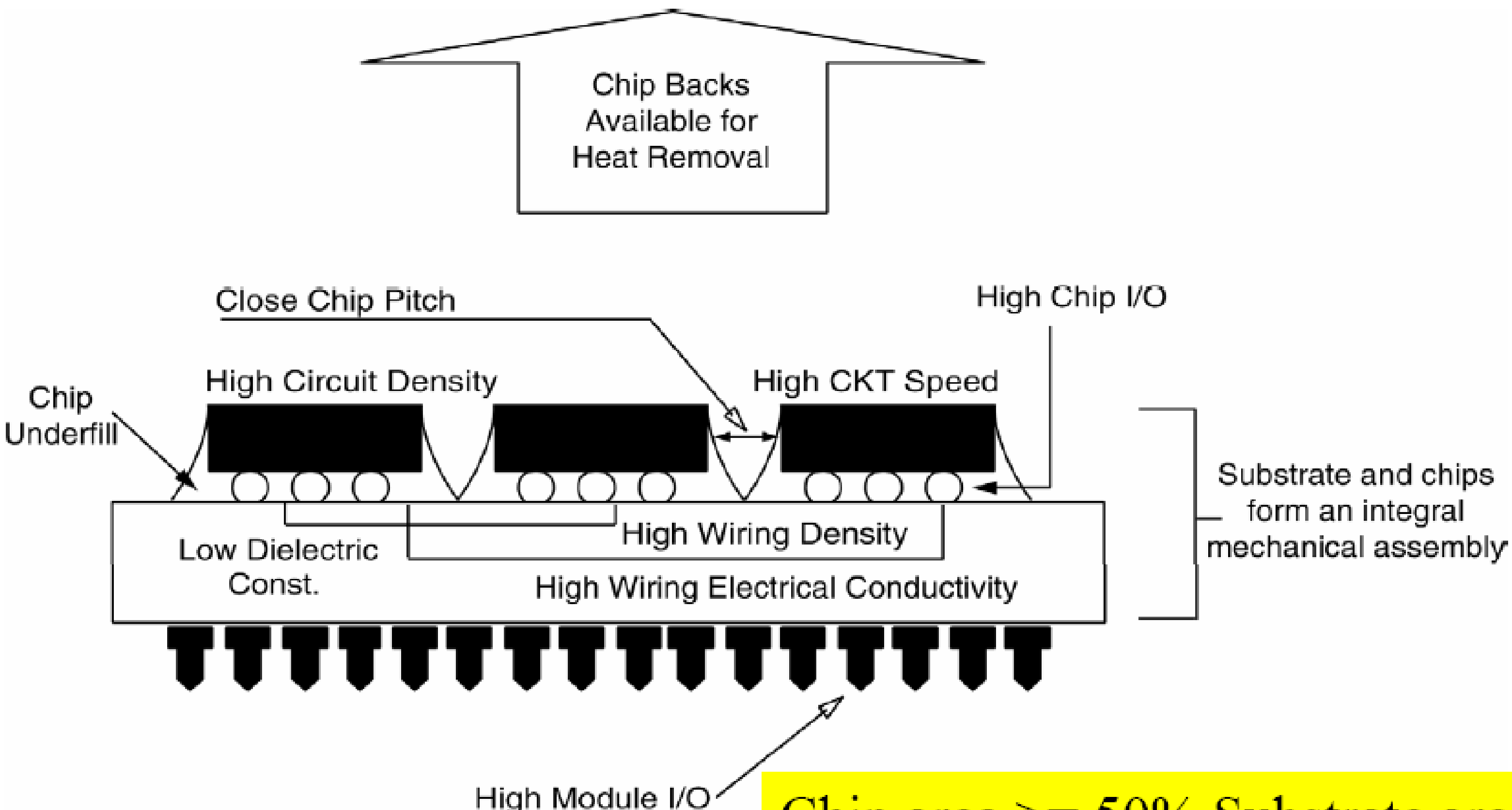
  Provide signal interconnect and I/O management

  - Thermal management
  - Mechanical support
  - Environmental protection

Multichip Module Functionality

- For a highly functional MCM, the following criteria must be satisfied:
  - Chip to chip spacing must be held to a minimum.
  - The MCM must provide a means of thermal management to limit the junction temperature of the semiconductor chips to less than 85 - 100°C.
  - The MCM must provide reliable I/O connections to the next level of assembly.
  - The MCM must provide protection from the environment.

Multichip Module Functionality

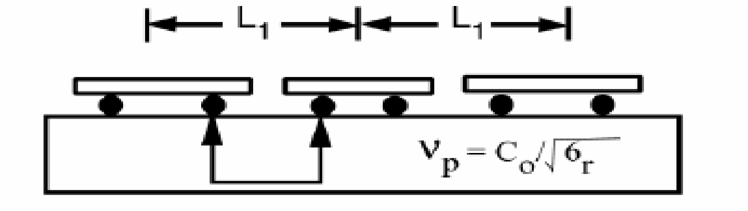


Chip area >= 50% Substrate area

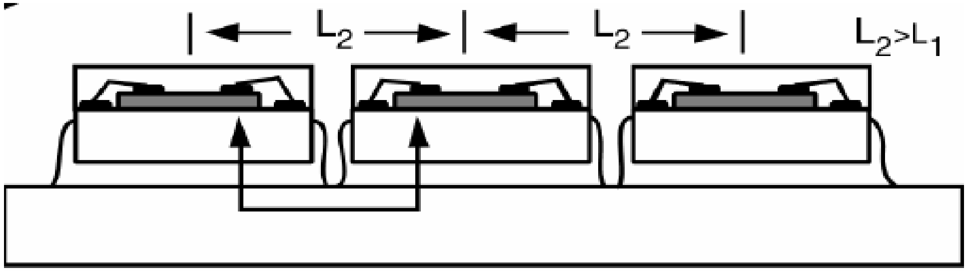
Packaging Efficiency

- Packaging efficiency is the ratio of the area of all the base chips to the area of the MCM substrate.
- Single chip package efficiency is between 10 – 50%.
- MCM package efficiency is around 80%.

Packaging Efficiency



MCM



Single Chips

Electrical Performance

- MCM performance can be measured by *functional throughput rate* (FTR).
  - FTR is the product of the number of gates per module times the maximum clock rate of such gates.
  - Maximum clock rate is $0.25t_D$ where t_D is the delay associated with the typical gate.
- Another measure of performance is MIPS.
  - Number of MIPS = 10^3 / [(cycle time) X (cycles per instructions)]
- Other measures include clock speed, operation frequency, and power dissipation.

Cost

- Cost is expected to be lower than the alternative single chip package implementation.

  Reduction of the number of interconnects and minimized substrate area and system volume.

- Cost per unit area is higher, but the overall size is smaller.

Electrical Design

- Considerations

  Signal paths must be short with controlled impedances and low loss.

  Deviations from design specifications can result in crosstalk, increased delays, and distorted signal waveforms.

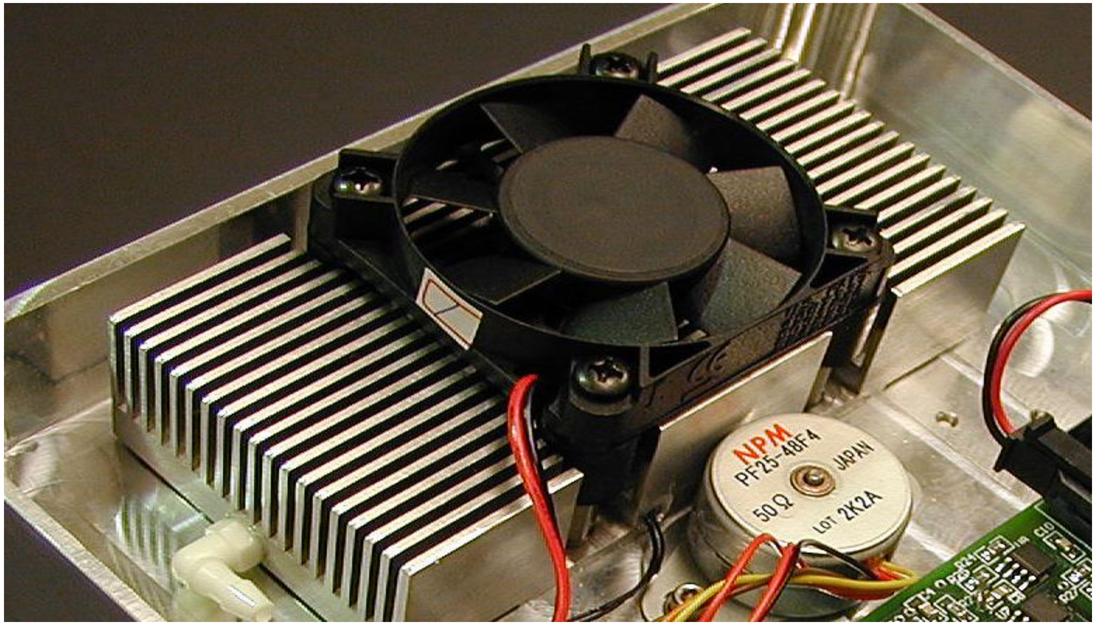
  Must address dielectric constant, signal line geometries, interline spacing, and the distribution and location of power and ground.

Sealing and Encapsulation

- MCMs are either hermetically sealed in ceramic or metal packages or they are encapsulated.
- Hermetic sealing or encapsulation of the MCM is important and can contribute to module reliability.
- Encapsulants need to be reworkable for high value MCMs.Encapsulant must be easy to remove.

Heat Removal

- Module power dissipations have risen from a few Watts per module to 30-180 Watts per module.
- ICs must be maintained at 100°C or below.



Heat Removal

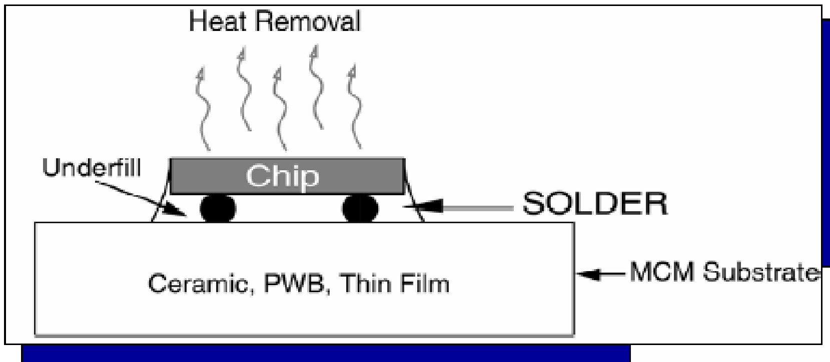
- Substrate aids in the heat removal process.
- Actual thermal transfer depends on how the chips are interconnected to the substrate.
- Three methods of interconnect:

  Wirebonding

  Flip Chip

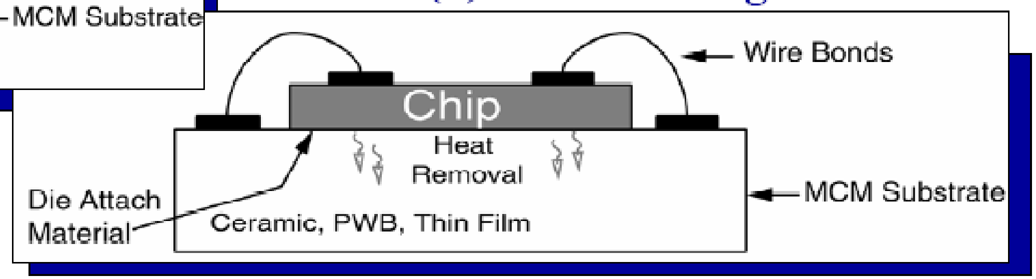
  Tape Automated Bonding (TAB)

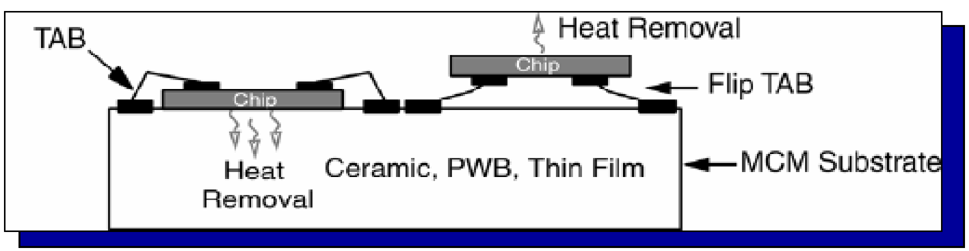
Heat Removal



(a) flip chip

(b) wire bonding





(c) tape automated bonding (TAB)

Electrical Interconnections

- **Requirements**

  Fatigue and creep resistance

  Corrosion resistance

  Electromigration resistance

  High conductivity

Electrical Interconnections

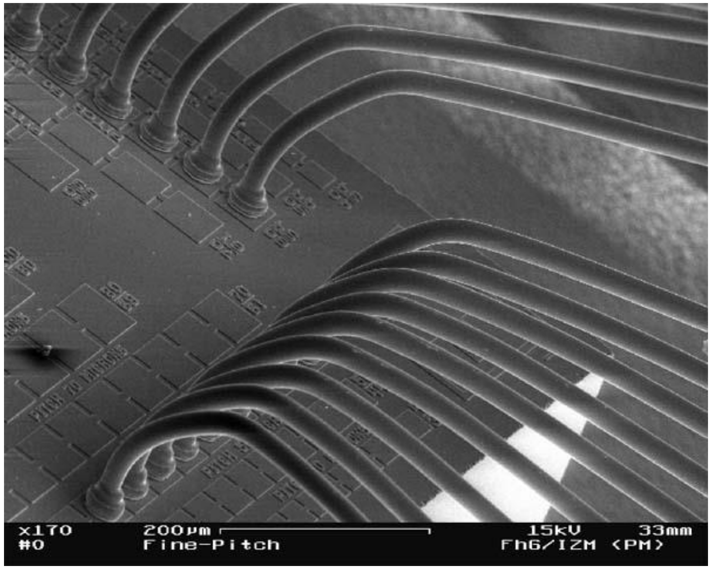
- **Wirebonding**

  Flexible

  Low interconnect cost

  Lower capitalization cost

  Ease of use



Electrical Testing

Different Levels of Testing

- Substrates must be defect free prior to assembly.
  - Verify that all networks are connected appropriately.
  - Visual inspection.
- After assembly, MCM must be electrically tested to ensure that the module is working.
  - Device must be encapsulated and environmentally stressed.

In an MCM, if one die fails, the whole module fails.

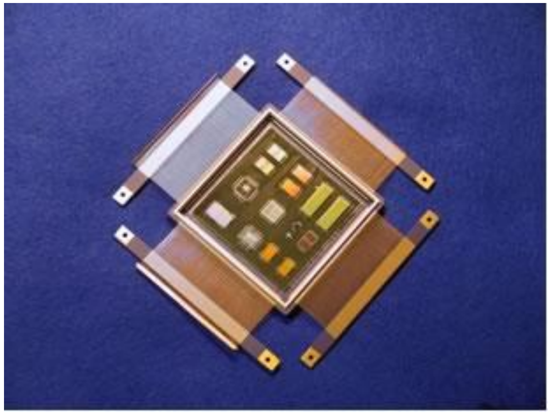
Types of Multichip Module Substrates

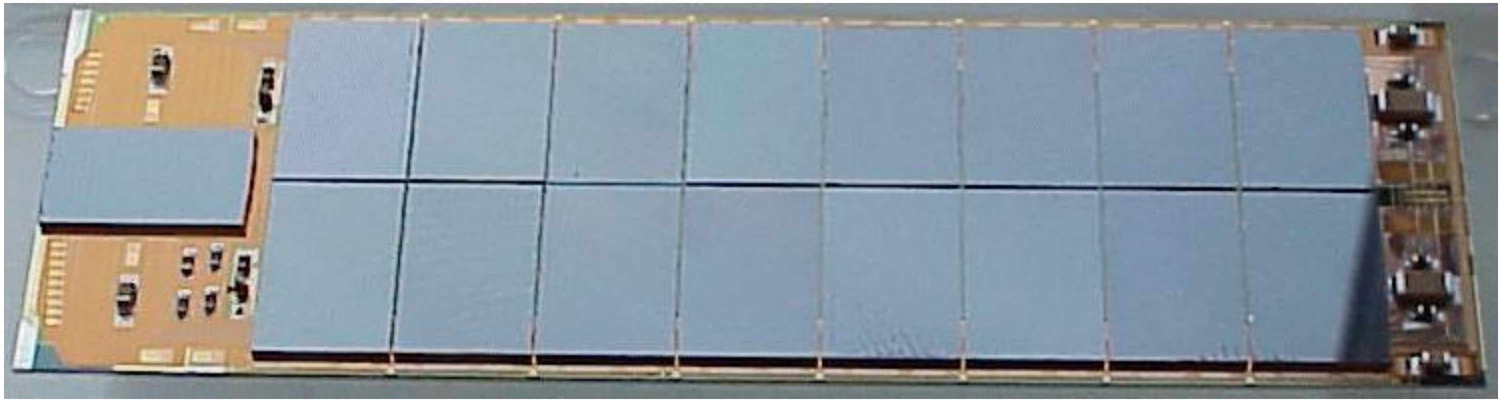
- MCM - More than half of its area covered with active devices
- Move from PWB to MCMs
- Three basic styles of MCMs

  MCM-L

  MCM-C

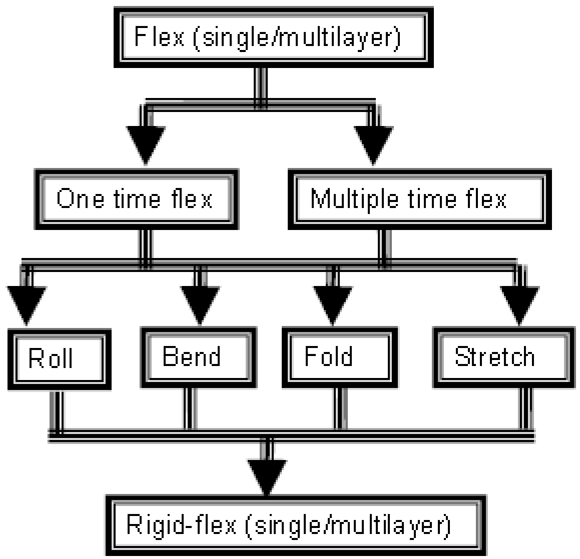
  MCM-D

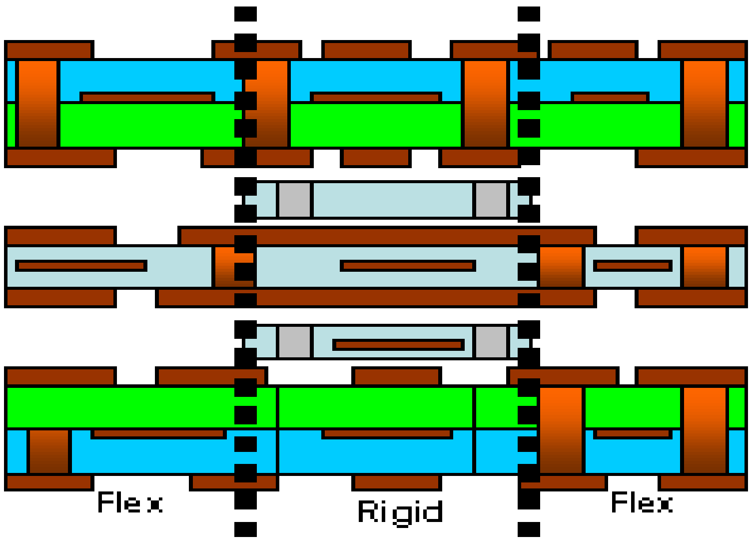




MCM-L

- Organic PWB fabrication
- Organic coatings used to protect chips and bonds
- Three types of lamination substrates
  - Rigid
  - Flex
  - Rigid flex


Flex (single/multilayer)
One time flex
Multiple time flex
Roll
Bend
Fold
Stretch
Rigid-flex (single/multilayer)


Flex
Rigid
Flex

MCM-L (continued)

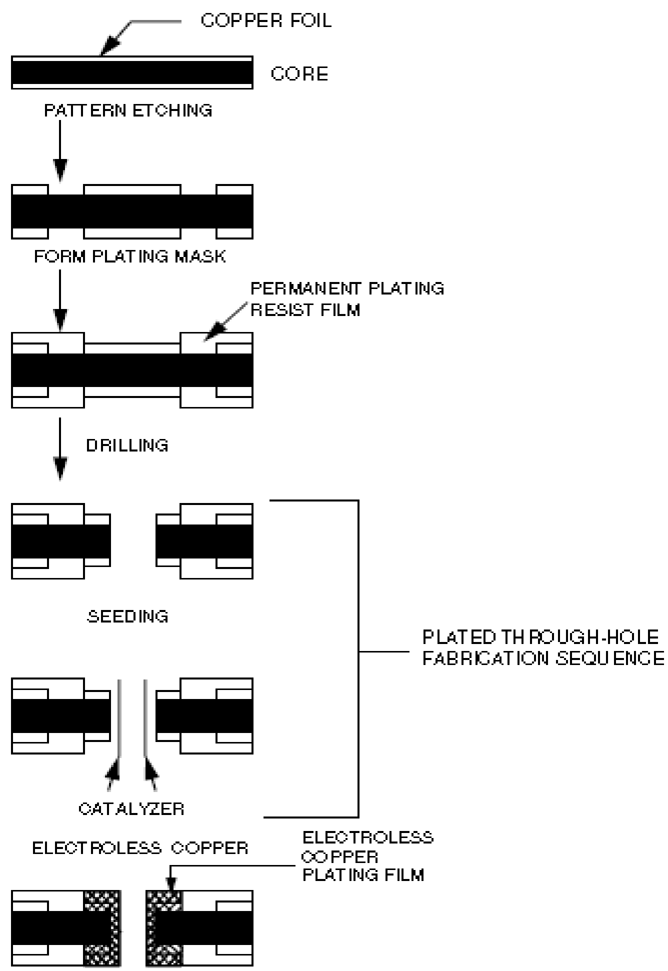
- Two types of dielectric layers in MCM-L construction
  - Cores
  - Prepregs
- **MCM-L substrate process**

  Selecting appropriate core and prepreg layers

  Photolithographic pattering and etching of copper conductors on the core layers

  Drilling of vias

  Lamination of the cores to each other using the prepreg layers.Plating of drilled holes in single layers, partially though several layers and holes all the way though the board

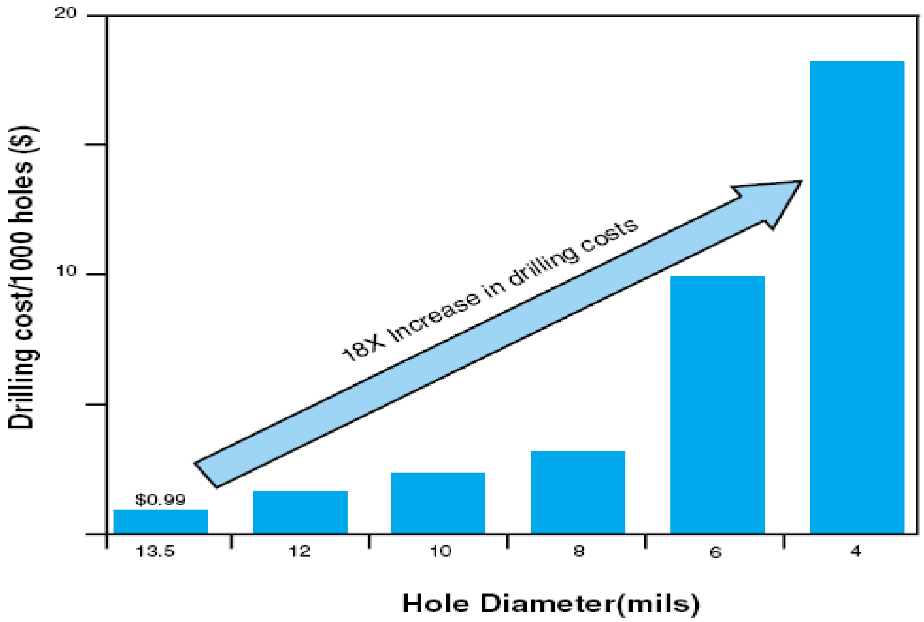

COPPER FOIL
CORE
PATTERN ETCHING
FORM PLATING MASK
PERMANENT PLATING
RESIST FILM
DRILLING
SEEDING
PLATED THROUGH-HOLE
FABRICATION SEQUENCE
CATALYZER
ELECTROLESS COPPER
ELECTROLESS
COPPER
PLATING FILM

MCM-L (continued)

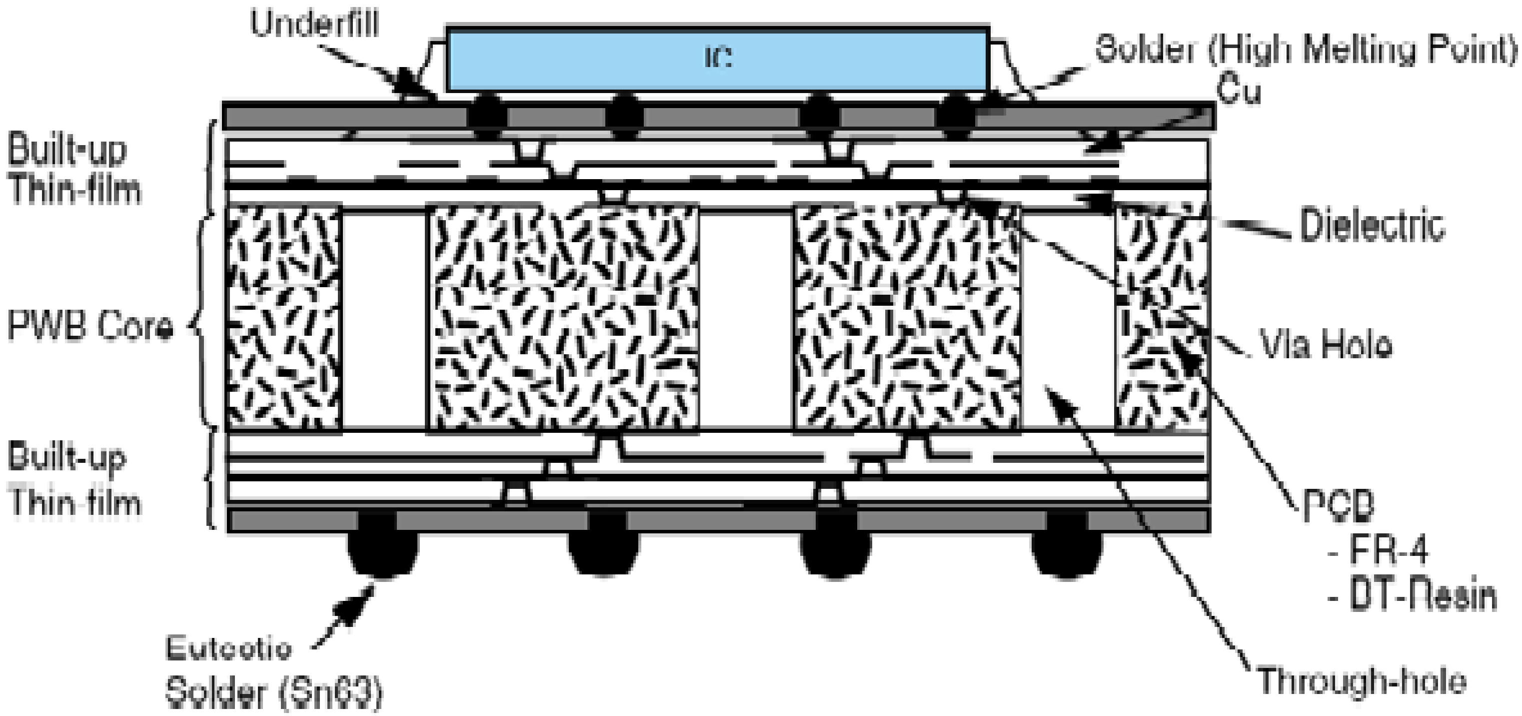
- Inner layer processing
  - Copper surfaces cleaned in preparation for pattern processing
  - Photo resist is applied by laminating of a dry film resist material (other techniques)
  - Liquid resists typically allow finer line definition
  - Pattern is exposed with ultraviolet light – removes unwanted resist areas
  - Copper foil is etched in ammonia-based alkaline system
  - Photoresist is chemically removed

Advanced MCM-L substrates

- Advanced MCM-L substrates
  - Cost increases as hole diameter decreases
  - In high density applications (micro processors) loss of wiring density cannot be tolerated
  - Built-up technology



Advanced MCM-L substrates



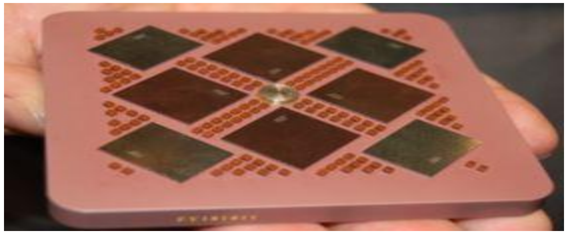
MCM-C

- Ceramic-based substrates
- Evolved from traditional thick-film fabrication techniques
- Density increased:

  Shrinking size of features (vias) used for interconnecting layers

  Shrinking conductor traces used for signal routing

  Shrinking gaps between traces or vias



MCM-C (continued)

- MCM-C Process

  Dielectric layers are sheets of unfired ceramic green state ceramic.Each sheet is separately patterned.

  Vias are mechanically punched or laser drilled.

  Vias filled by extruding the conducting paste into the holes though a stencil.

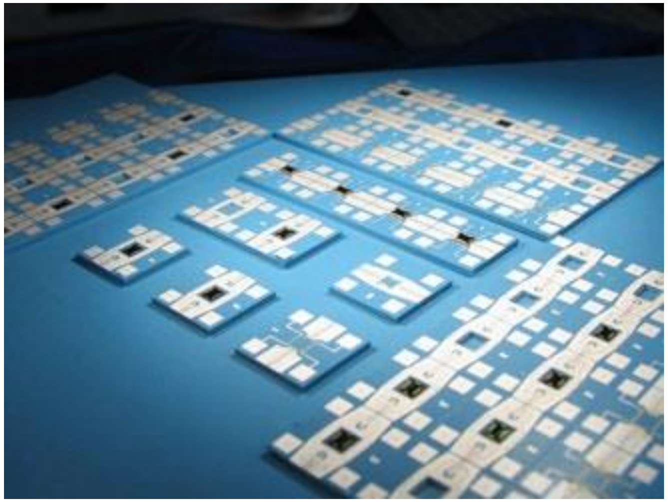
  Fired.

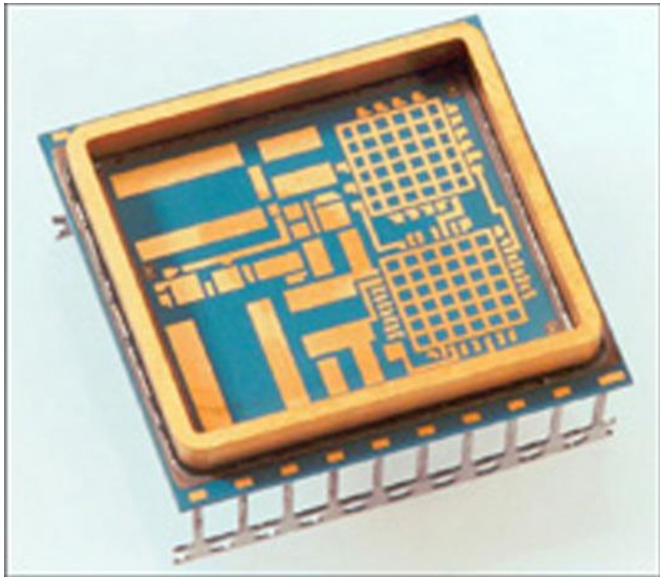
MCM-C (continued)

- 2 –types

  High temperature cofired ceramic (HTCC)

  Low temperature cofired ceramic (LTCC)





MCM-D

- Combination of superior materials and dimensional resolving power of thin-film technology
- Several dielectric/metallization technologies
- Vias are formed in the polyimide by reactive-ion etching in an oxygen plasma using a photo-patterned metal mask

Multichip Module Design

- Wireability analysis used to find the basic size possible
- Basic concepts

  Estimation of wiring demand

  Wiring capacity

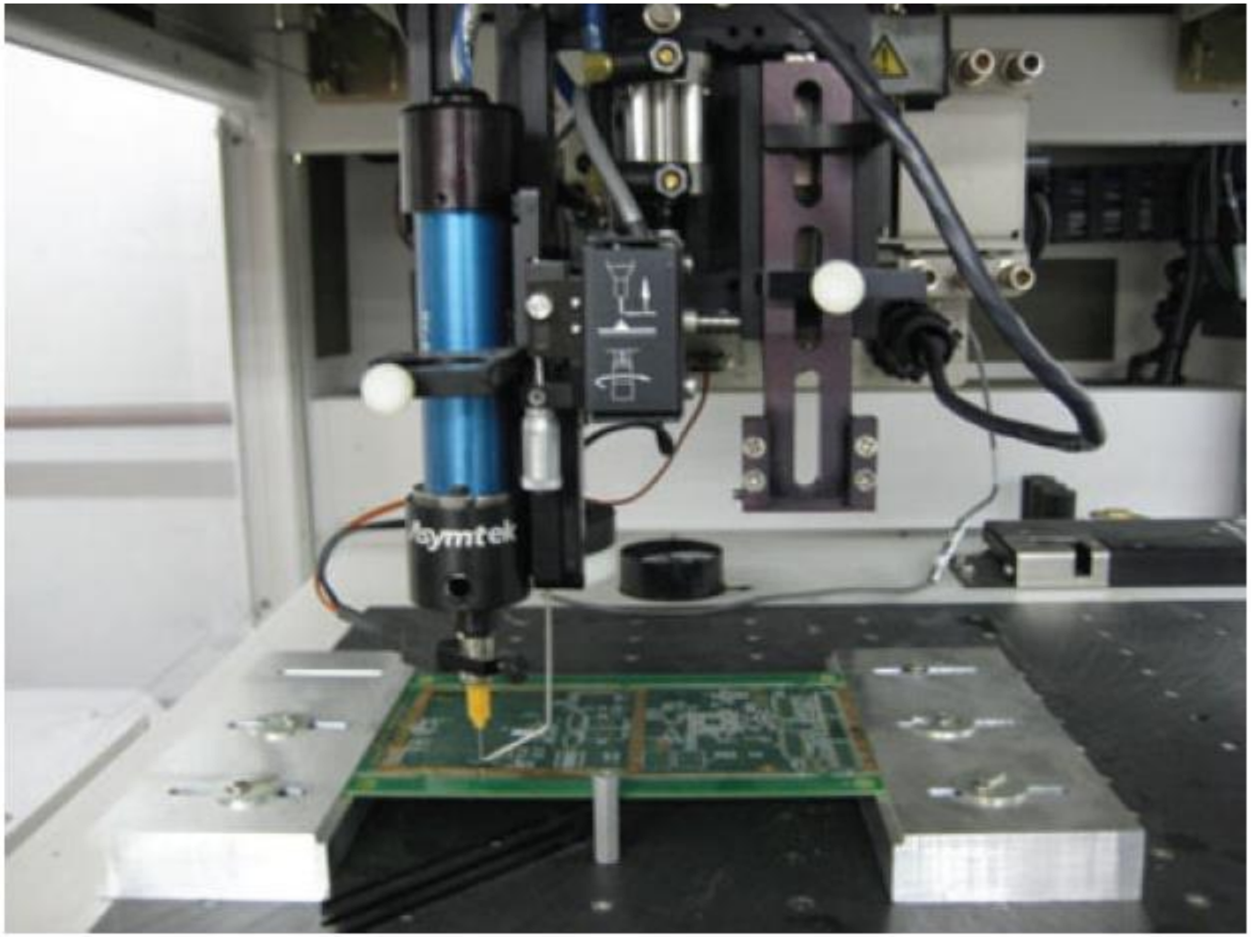
  Average wire length

  Connectivity

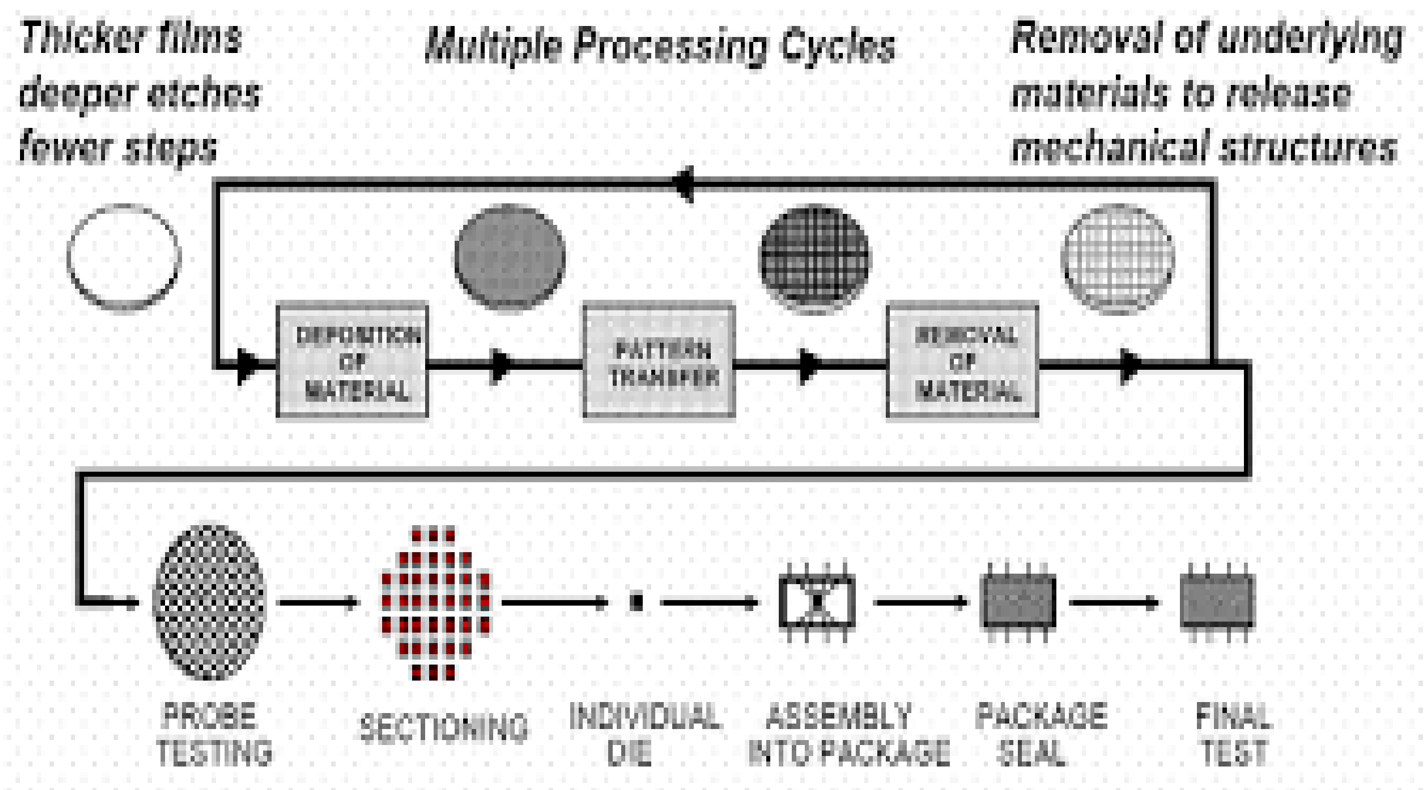
Multichip Module Design (continued)

- Wiring demand (D) amount of wiring required to interconnect a given circuit
- Wiring capability (C) is the amount of wiring available for interconnection
- Wiring efficiency 30-70% range depending on circuit type

$$D = \varepsilon C$$



Picture courtesy of Nexlogic.


Thicker films
deeper etches
fewer steps
Multiple Processing Cycles
Removal of underlying
materials to release
mechanical structures
DEPOSITION
OF
MATERIAL
PATTERN
TRANSFER
REMOVAL
OF
MATERIAL
PROBE
TESTING
SECTIONING
INDIVIDUAL
DIE
ASSEMBLY
INTO PACKAGE
PACKAGE
SEAL
FINAL
TEST