## Complete 8086 instruction set

Quick reference:

|  | CMPSB |  |  |  | MOV |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AAA | CMPSW | JAE | JNBE | JPO | MOVSB | RCR | SCASB |
| AAD | CWD | JB | JNC | JS | MOVSW | REP | SCASW |
| AAM | DAA | JBE | JNE | JZ | MUL | REPE | SHL |
| AAS | DAS | JC | JNG | LAHF | NEG | REPNE | SHR |
| ADC | DEC | JCXZ | JNGE | LDS | NOP | REPNZ | STC |
| ADD | DIV | JE | JNL | LEA | NOT | REPZ | STD |
| AND | HLT | JG | JNLE | LES | OR | RET | STI |
| CALL | IDIV | JGE | JNO | LODSB | OUT | RETF | STOSB |
| CBW | IMUL | JL | JNP | LODSW | POP | ROL | STOSW |
| CLC | IN | JLE | JNS | LOOP | POPA | ROR | SUB |
| CLD | INC | JMP | JNZ | LOOPE | POPF | SAHF | TEST |
| CLI | INT | JNA | J0 | LOOPNE | PUSH | SAL | XCHG |
| CMC | INTO | JNAE | JP | LOOPNZ | PUSHA | SAR | XLATB |
| CMP | IRET | JNB | JPE | L00PZ | PUSHF | SBB | XOR |
|  | JA |  |  |  | RCL |  |  |

Operand types:
REG: AX, BX, CX, DX, AH, AL, BL, BH, CH, CL, DH, DL, DI, SI, BP, SP.
SREG: DS, ES, SS, and only as second operand: CS.
memory: [ $B X],[B X+S I+7]$, variable, etc...(see Memory Access).
immediate: 5, -24, 3Fh, 10001101b, etc...

## Notes:

- When two operands are required for an instruction they are separated by comma. For example:

REG, memory

- When there are two operands, both operands must have the same size (except shift and rotate instructions). For example:

AL, DL
DX, AX
m1 DB ?
AL, m1
m2 DW ?
AX, m2

- Some instructions allow several operand combinations. For example:
memory, immediate

REG, immediate
memory, REG
REG, SREG

- Some examples contain macros, so it is advisable to use Shift + F8 hot key to Step Over (to make macro code execute at maximum speed set step delay to zero), otherwise emulator will step through each instruction of a macro. Here is an example that uses PRINTN macro:

```
include 'emu8086.inc'
ORG 100h
MOV AL, 1
MOV BL, 2
PRINTN 'Hello World!' ; macro.
MOV CL, 3
PRINTN 'Welcome!' ; macro.
RET
```

These marks are used to show the state of the flags:
1 - instruction sets this flag to $\mathbf{1}$.
$\mathbf{0}$ - instruction sets this flag to $\mathbf{0}$.
$\mathbf{r}$ - flag value depends on result of the instruction.
? - flag value is undefined (maybe $\mathbf{1}$ or $\mathbf{0}$ ).

Some instructions generate exactly the same machine code, so disassembler may have a problem decoding to your original code. This is especially important for Conditional Jump instructions (see "Program Flow Control" in Tutorials for more information).

Instructions in alphabetical order:

| Instruction | Operands | Description |
| :---: | :---: | :---: |
|  |  | ASCII Adjust after Addition. <br> Corrects result in AH and AL after addition when working with BCD values. <br> It works according to the following Algorithm: <br> if low nibble of $\mathrm{AL}>9$ or $\mathrm{AF}=1$ then: |


| AAA | No operands | - $A L=A L+6$ <br> - $A H=A H+1$ <br> - $A F=1$ <br> - $C F=1$ <br> else <br> - $\mathrm{AF}=0$ <br> - $C F=0$ <br> in both cases: <br> clear the high nibble of AL. <br> Example: $\begin{array}{ll} \text { MOV } A X, 15 ; & A H=00, A L=0 F h \\ \text { AAA } & ; A H=01, A L=05 \end{array}$ <br> RET |
| :---: | :---: | :---: |
| AAD | No operands | ASCII Adjust before Division. <br> Prepares two BCD values for division. <br> Algorithm: <br> - $A L=(A H * 10)+A L$ <br> - $A H=0$ <br> Example: $\begin{array}{ll} \operatorname{Mov} A X, ~ 0105 h & ; A H=01, A L=05 \\ \text { AAD } & ; A H=00, A L=0 F h \tag{15} \end{array}$ <br> RET |
|  |  | ASCII Adjust after Multiplication. Corrects the result of multiplication of two BCD values. <br> Algorithm: <br> - AH = AL / 10 <br> - AL = remainder |


| AAM | No operands | Example: $\begin{array}{ll} \text { MOV AL, } 15 & ; A L=0 F h \\ \text { AAM } & ; A H=01, A L=05 \end{array}$ <br> RET |
| :---: | :---: | :---: |
| AAS | No operands | ASCII Adjust after Subtraction. Corrects result in AH and AL after subtraction when working with BCD values. <br> Algorithm: <br> if low nibble of $A L>9$ or $A F=1$ then: <br> - $A L=A L-6$ <br> - AH = AH - 1 <br> - $\mathrm{AF}=1$ <br> - $C F=1$ <br> else <br> - $A F=0$ <br> - CF $=0$ <br> in both cases: <br> clear the high nibble of AL. <br> Example: $\begin{aligned} & \text { MOV AX, 02FFh } \\ & \text { AAS } \\ & \text { RET } \end{aligned}$ |
| ADC | REG, memory memory, REG REG, REG | Add with Carry. <br> Algorithm: <br> operand1 $=$ operand1 + operand $2+$ CF <br> Example: |


|  | memory, immediate REG, immediate | STC MOV AL, $5 ;$ set CF $=1$ ADC AL, $1 ;$ RET |
| :---: | :---: | :---: |
| ADD | REG, memory <br> memory, REG <br> REG, REG <br> memory, immediate <br> REG, immediate | Add. <br> Algorithm: <br> operand1 $=$ operand1 + operand2 <br> Example: <br> $\begin{array}{ll}\text { MOV } A L, 5 & ; A L=5 \\ \text { ADD } A L,-3 & ; A L=2\end{array}$ <br> RET |
| AND | REG, memory memory, REG REG, REG memory, immediate REG, immediate | Logical AND between all bits of two operands. Result is stored in operand1. <br> These rules apply: <br> 1 AND $1=1$ <br> 1 AND $0=0$ <br> 0 AND $1=0$ <br> 0 AND $0=0$ <br> Example: $\begin{array}{ll} \text { MOV AL, 'a' } & ; A L=01100001 b \\ \text { AND } A L, ~ 11011111 b ~ & ; A L=01000001 b \quad(' A ') \end{array}$ <br> RET |
|  |  | Transfers control to procedure, return address is (IP) is pushed to stack. 4-byte address may be entered in this form: 1234h:5678h, first value is a |


| CALL | procedure name label <br> 4-byte address | segment second value is an offset (this is a far call, so CS is also pushed to stack). <br> Example: <br> ORG 100h ; for COM file. <br> CALL p1 <br> ADD AX, 1 <br> RET ; return to OS. <br> p1 PROC ; procedure declaration. <br> MOV AX, 1234h <br> RET ; return to caller. <br> p1 ENDP |
| :---: | :---: | :---: |
| CBW | No operands | Convert byte into word. <br> Algorithm: <br> if high bit of $A L=1$ then: <br> - $\mathrm{AH}=255$ (0FFh) <br> else <br> - $\mathrm{AH}=0$ <br> Example: $\begin{array}{ll} \text { MOV AX, } 0 & ; A H=0, A L=0 \\ \text { MOV AL, }-5 & ; A X=000 F B h(251) \\ \text { CBW } & ; A X=0 F F F B h(-5) \\ \text { RET } & \end{array}$ |
|  |  | Clear Carry flag. <br> Algorithm: $C F=0$ |


| CLC | No operands | $\begin{array}{\|c\|} \hline \mathrm{C} \\ \hline 0 \\ \hline \end{array}$ |
| :---: | :---: | :---: |
| CLD | No operands | Clear Direction flag. SI and DI will be incremented by chain instructions: CMPSB, CMPSW, LODSB, LODSW, MOVSB, MOVSW, STOSB, STOSW. <br> Algorithm: $D F=0$ $\begin{array}{\|l\|l\|} \hline \text { D } \\ \hline 0 \\ \hline \end{array}$ |
| CLI | No operands | Clear Interrupt enable flag. This disables hardware interrupts. <br> Algorithm: $\text { IF }=0$ |
| CMC | No operands | Complement Carry flag. Inverts value of CF. <br> Algorithm: <br> if $C F=1$ then $C F=0$ <br> if $C F=0$ then $C F=1$ $\square$ |
|  |  | Compare. <br> Algorithm: <br> operand1 - operand2 |


| CMP | REG, memory memory, REG REG, REG memory, immediate REG, immediate | result is not stored anywhere, flags are set (OF, SF, ZF, AF, PF, CF) according to result. <br> Example: <br> MOV AL, 5 <br> MOV BL, 5 <br> CMP AL, BL ; $\mathrm{AL}=5, \mathrm{ZF}=1$ (so equal!) <br> RET |
| :---: | :---: | :---: |
| CMPSB | No operands | Compare bytes: ES:[DI] from DS:[SI]. <br> Algorithm: ```- DS:[SI] - ES:[DI] - set flags according to result: OF, SF, ZF, AF, PF, CF - if DF = 0 then - SI = SI + 1 DI = DI + 1 else SI = SI - 1 DI = DI - 1``` <br> Example: open cmpsb.asm from c:\emu8086\examples |
| CMPSW | No operands | Compare words: ES:[DI ] from DS:[SI]. <br> Algorithm: ```- DS:[SI] - ES:[DI] - set flags according to result: OF, SF, ZF, AF, PF, CF - if DF \(=0\) then - SI = SI + 2 - DI = DI + 2 else SI = SI - 2 DI = DI - 2``` |


|  |  | example: open cmpsw.asm from c:\emu8086\examples |
| :---: | :---: | :---: |
| CWD | No operands | Convert Word to Double word. <br> Algorithm: <br> if high bit of $A X=1$ then: <br> - $D X=65535$ (0FFFFh) <br> else <br> - $D X=0$ <br> Example: |
| DAA | No operands | Decimal adjust After Addition. <br> Corrects the result of addition of two packed BCD values. <br> Algorithm: <br> if low nibble of $A L>9$ or $A F=1$ then: <br> - $A L=A L+6$ <br> - $A F=1$ <br> if AL > 9Fh or CF = 1 then: <br> - $A L=A L+60 h$ <br> - $C F=1$ <br> Example: |



| DIV | REG memory | Unsigned divide. <br> Algorithm: <br> when operand is a byte: <br> AL = AX / operand <br> AH = remainder (modulus) <br> when operand is a word: <br> $A X=(D X A X) /$ operand <br> DX = remainder (modulus) <br> Example: <br> MOV AX, 203 ; AX = 00CBh <br> MOV BL, 4 <br> DIV BL $\quad ; A L=50(32 h), A H=3$ <br> RET |
| :---: | :---: | :---: |
| HLT | No operands | Halt the System. <br> Example: <br> MOV AX, 5 <br> HLT |
| IDIV | REG memory | Signed divide. <br> Algorithm: <br> when operand is a byte: <br> AL = AX / operand <br> AH = remainder (modulus) <br> when operand is a word: <br> $A X=(D X A X) /$ operand <br> DX = remainder (modulus) <br> Example: <br> MOV AX, -203 ; AX = 0FF35h <br> MOV BL, 4 <br> IDIV BL ; AL = -50 (0CEh), $A H=-3$ (0FDh) <br> RET |


|  |  | C $Z$ $S$ 0 $P$ <br> $?$ $A$    <br> $?$ $?$ $?$ $?$ $?$ |
| :---: | :---: | :---: |
| IMUL | REG memory | Signed multiply. <br> Algorithm: <br> when operand is a byte: <br> AX = AL * operand. <br> when operand is a word: <br> $(D X A X)=A X$ * operand. <br> Example: <br> MOV AL, -2 <br> MOV BL, -4 <br> IMUL BL ; AX = 8 <br> RET <br> $\mathrm{CF}=0 \mathrm{~F}=0$ when result fits into operand of IMUL. |
| IN | AL, im.byte <br> AL, DX <br> AX, im.byte <br> AX, DX | Input from port into $\mathbf{A L}$ or $\mathbf{A X}$. Second operand is a port number. If required to access port number over 255 - DX register should be used. <br> Example: <br> IN AX, 4 ; get status of traffic lights. <br> IN AL, 7 ; get status of stepper-motor. <br> unchanged |
| INC | REG memory | Increment. <br> Algorithm: <br> operand = operand + 1 <br> Example: $\begin{aligned} & \text { MOV AL, } 4 \\ & \text { INC AL } \quad ; A L=5 \end{aligned}$ |







| JE | label | Signed/Unsigned. <br> Algorithm: <br> if $Z F=1$ then jump <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV AL, 5 <br> CMP AL, 5 <br> JE label1 <br> PRINT 'AL is not equal to 5.' <br> JMP exit <br> label1: <br> PRINT 'AL is equal to 5.' <br> exit: <br> RET <br> unchanged |
| :---: | :---: | :---: |
| JG | label | Short Jump if first operand is Greater then second operand (as set by CMP instruction). Signed. <br> Algorithm: <br> if ( $\mathrm{ZF}=0$ ) and $(\mathrm{SF}=0 \mathrm{~F})$ then jump <br> Example: ```include 'emu8086.inc' ORG 100h MOV AL, 5 CMP AL, -5 JG label1 PRINT 'AL is not greater -5.' JMP exit label1: PRINT 'AL is greater -5.' RET``` exit: CZ Z S O P A unchanged |
|  |  | Short Jump if first operand is Greater or Equal to second operand (as set by CMP instruction). Signed. <br> Algorithm: |





|  |  | ```JMP exit label1: PRINT 'AL >= 5.' exit: RET```  |
| :---: | :---: | :---: |
| JNBE | label | Short Jump if first operand is Not Below and Not Equal to second operand (as set by CMP instruction). Unsigned. <br> Algorithm: <br> if ( $C F=0$ ) and ( $Z F=0$ ) then jump <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV AL, 7 <br> CMP AL, 5 <br> JNBE label1 <br> PRINT 'AL <= 5.' <br> JMP exit <br> label1: <br> PRINT 'AL > 5.' <br> exit: <br> RET <br> unchanged |
| JNC | label | Short Jump if Carry flag is set to 0 . <br> Algorithm: <br> if $C F=0$ then jump <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV AL, 2 <br> ADD AL, 3 <br> JNC label1 <br> PRINT 'has carry.' <br> JMP exit <br> label1: <br> PRINT 'no carry.' <br> exit: |





## Short Jump if Not Overflow.

Algorithm:

$$
\text { if } O F=0 \text { then jump }
$$

## Example:

```
    ; -5 - 2 = -7 (inside -128..127)
    ; the result of SUB is correct,
    ; so OF = 0:
    include 'emu8086.inc'
    ORG 100h
    MOV AL, -5
    SUB AL, 2 ; AL = 0F9h (-7)
    JNO label1
    PRINT 'overflow!'
    JMP exit
    label1:
    PRINT 'no overflow.'
    exit:
        RET
    C|SOPA
```



Short Jump if Not Signed (if positive). Set by CMP, SUB, ADD, TEST, AND, OR, XOR instructions.

Algorithm:

```
if SF = 0 then jump
```


## Example:

include 'emu8086.inc'
ORG 100h
MOV AL, 00000111b ; AL = 7
OR AL, 0 ; just set flags.
JNS label1
PRINT 'signed.'
JMP exit
label1:
PRINT 'not signed.'
exit:
RET
unchanged

|  |  |  |
| :---: | :---: | :---: |
| JNZ | label | Short Jump if Not Zero (not equal). Set by CMP, SUB, ADD, TEST, AND, OR, XOR instructions. <br> Algorithm: <br> if $\mathrm{ZF}=0$ then jump <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV AL, 00000111b ; AL = 7 <br> OR AL, 0 ; just set flags. <br> JNZ label1 <br> PRINT 'zero.' <br> JMP exit <br> label1: <br> PRINT 'not zero.' <br> exit: <br> RET <br> unchanged |
| J0 | label | Short Jump if Overflow. <br> Algorithm: <br> if $O F=1$ then jump <br> Example: ```; -5 - 127 = -132 (not in -128..127) ; the result of SUB is wrong (124), ; so OF = 1 is set: include 'emu8086.inc' org 100h MOV AL, -5 SUB AL, 127 ; AL = 7Ch (124) j0 label1 PRINT 'no overflow.' JMP exit label1: PRINT 'overflow!' exit: RET``` |


| JP | label | Short Jump if Parity (even). Only 8 low bits of result are checked. Set by CMP, SUB, ADD, TEST, AND, OR, XOR instructions. <br> Algorithm: <br> if $\mathrm{PF}=1$ then jump <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV AL, 00000101b ; AL = 5 <br> OR AL, 0 ; just set flags. <br> JP label1 <br> PRINT 'parity odd.' <br> JMP exit <br> label1: <br> PRINT 'parity even.' <br> exit: <br> RET <br> unchanged |
| :---: | :---: | :---: |
| JPE | label | Short Jump if Parity Even. Only 8 low bits of result are checked. Set by CMP, SUB, ADD, TEST, AND, OR, XOR instructions. <br> Algorithm: <br> if $P F=1$ then jump <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV AL, 00000101b ; AL = 5 <br> OR AL, 0 ; just set flags. <br> JPE label1 <br> PRINT 'parity odd.' <br> JMP exit <br> label1: <br> PRINT 'parity even.' <br> exit: <br> RET <br> unchanged |
|  |  | Short Jump if Parity Odd. Only 8 low bits of result |



| JZ | label | Algorithm: <br> if $Z F=1$ then jump <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV AL, 5 <br> CMP AL, 5 <br> JZ label1 <br> PRINT 'AL is not equal to 5.' <br> JMP exit <br> label1: <br> PRINT 'AL is equal to 5.' <br> exit: <br> RET |
| :---: | :---: | :---: |
| LAHF | No operands | Load AH from 8 low bits of Flags register. <br> Algorithm: AH = flags register <br>  bits 1, 3, 5 are reserved. <br> unchanged |
|  |  | Load memory double word into word register and DS. <br> Algorithm: <br> - REG = first word <br> - DS = second word <br> Example: <br> ORG 100h |


| LDS | REG, memory | LDS AX, m <br> RET <br> $\begin{array}{lll}\text { m } & \text { DW } & \text { 1234h } \\ & \text { DW } & 5678 \mathrm{~h}\end{array}$ <br> END <br> AX is set to $1234 \mathrm{~h}, \mathrm{DS}$ is set to 5678 h . |
| :---: | :---: | :---: |
| LEA | REG, memory | Load Effective Address. <br> Algorithm: <br> - REG = address of memory (offset) <br> Example: <br> MOV BX, 35h <br> MOV DI, 12h <br> LEA SI, [BX+DI] ; SI = 35h + 12h = 47h <br> Note: The integrated 8086 assembler automatically replaces LEA with a more efficient MOV where possible. For example: <br> org 100h <br> LEA AX, m ; AX = offset of m <br> RET <br> m dw 1234h <br> END |
|  |  | Load memory double word into word register and ES. <br> Algorithm: |



|  |  |  |
| :---: | :---: | :---: |
| LODSW | No operands | Load word at DS:[SI] into AX. Update SI. <br> Algorithm: <br> - AX = DS:[SI] <br> - if DF = 0 then <br> - SI = SI + 2 <br> else <br> - SI = SI - 2 <br> Example: <br> ORG 100h <br> LEA SI, a1 <br> MOV CX, 5 <br> REP LODSW ; finally there will be 555h in AX. <br> RET <br> a1 dw 111h, 222h, 333h, 444h, 555h $\square$ <br> C\|Z|S|O|S| <br> unchanged |
| LOOP | label | Decrease CX, jump to label if CX not zero. <br> Algorithm: <br> - CX = CX - 1 <br> - if CX <> 0 then <br> - jump <br> else <br> - no jump, continue <br> Example: <br> include 'emu8086.inc' <br> ORG 100h <br> MOV CX, 5 <br> label1: <br> PRINTN 'loop!' <br> LOOP label1 <br> RET <br> unchanged |


|  |  |  |
| :---: | :---: | :---: |
| LOOPE | label | Decrease CX, jump to label if CX not zero and Equal ( $Z F=1$ ). <br> Algorithm: <br> - CX = CX - 1 <br> - if (CX <> 0) and (ZF = 1) then - jump <br> else <br> - no jump, continue <br> Example: ```; Loop until result fits into AL alone, ; or 5 times. The result will be over 255 ; on third loop (100+100+100), ; so loop will exit. include 'emu8086.inc' ORG 100h MOV AX, 0 MOV CX, 5 label1: PUTC '*' ADD AX, 100 CMP AH, 0 LOOPE label1 RET CZSOPA unchanged``` |




| LOOPZ | label | ```- if (CX <> 0) and (ZF = 1) then - jump else \circ no jump, continue``` <br> Example: ```Loop until result fits into AL alone, or 5 times. The result will be over 255 on third loop (100+100+100), so loop will exit. include 'emu8086.inc' ORG 100h MOV AX, 0 MOV CX, 5 label1: PUTC '*' ADD AX, 100 CMP AH, 0 LOOPZ label1 RET``` |
| :---: | :---: | :---: |
| MOV | REG, memory memory, REG REG, REG memory, immediate REG, immediate <br> SREG, memory memory, SREG REG, SREG SREG, REG | Copy operand2 to operand1. <br> The MOV instruction cannot: <br> - set the value of the CS and IP registers. <br> - copy value of one segment register to another segment register (should copy to general register first). <br> - copy immediate value to segment register (should copy to general register first). <br> Algorithm: operand1 = operand2 <br> Example: |



| MOVSW | No operands | ```ORG 100h \\ CLD \\ LEA SI, a1 \\ LEA DI, a2 \\ MOV CX, 5 \\ REP MOVSW \\ RET \\ a1 DW 1,2,3,4,5 \\ a2 DW \(5 \operatorname{DUP}(0)\)```CDS $\mathrm{S}\|\mathrm{P}\|$ <br> unchanged |
| :---: | :---: | :---: |
| MUL | REG memory | Unsigned multiply. <br> Algorithm: <br> when operand is a byte: <br> AX = AL * operand. <br> when operand is a word: <br> $(D X A X)=A X$ * operand. <br> Example: $\begin{array}{ll} \text { MOV AL, } 200 & ; A L=0 C 8 h \\ \text { MOV BL, } 4 & \\ \text { MUL BL } & ; A X=0320 h(800) \\ \text { RET } & \end{array}$  <br> $\mathrm{CF}=\mathrm{OF}=0$ when high section of the result is zero. |
| NEG | REG memory | Negate. Makes operand negative (two's complement). <br> Algorithm: <br> - Invert all bits of the operand <br> - Add 1 to inverted operand <br> Example: |



| OR | memory, REG <br> REG, REG <br> memory, immediate <br> REG, immediate | Example: RET |
| :---: | :---: | :---: |
| OUT | im.byte, AL <br> im.byte, AX <br> DX, AL <br> DX, AX | Output from AL or AX to port. <br> First operand is a port number. If required to access port number over 255 - DX register should be used. <br> Example: <br> MOV AX, 0FFFh ; Turn on all <br> OUT 4, AX ; traffic lights. <br> MOV AL, 100b ; Turn on the third <br> OUT 7, AL ; magnet of the stepper-motor. |
| POP | REG <br> SREG <br> memory | Get 16 bit value from the stack. <br> Algorithm: <br> - operand = SS:[SP] (top of the stack) <br> - $S P=S P+2$ <br> Example: <br> MOV AX, 1234h <br> PUSH AX <br> POP DX ; DX = 1234h <br> RET <br> CAS SOPA <br> unchanged |
|  |  | Pop all general purpose registers $\mathrm{DI}, \mathrm{SI}, \mathrm{BP}, \mathrm{SP}$, $\mathrm{BX}, \mathrm{DX}, \mathrm{CX}, \mathrm{AX}$ from the stack. |


| POPA | No operands | SP value is ignored, it is Popped but not set to SP register). <br> Note: this instruction works only on 80186 CPU and later! <br> Algorithm: <br> - POP DI <br> - POP SI <br> - POP BP <br> - POP xx (SP value ignored) <br> - POP BX <br> - POP DX <br> - POP CX <br> - POP AX |
| :---: | :---: | :---: |
| POPF | No operands | Get flags register from the stack. <br> Algorithm: <br> - flags = SS:[SP] (top of the stack) <br> - $S P=S P+2$ |
| PUSH | REG <br> SREG <br> memory <br> immediate | Store 16 bit value in the stack. <br> Note: PUSH immediate works only on 80186 <br> CPU and later! <br> Algorithm: <br> - $S P=S P-2$ <br> - SS:[SP] (top of the stack) = operand <br> Example: <br> MOV AX, 1234h <br> PUSH AX <br> POP DX ; DX = 1234h <br> RET |




| REP | chain instruction | - CX = CX - 1 <br> - go back to check_cx else <br> - exit from REP cycle $\square$ |
| :---: | :---: | :---: |

|REPE

Repeat following CMPSB, CMPSW, SCASB, SCASW instructions while ZF $=1$ (result is Equal), maximum CX times.

Algorithm:
check_cx:
if CX <> 0 then

- do following chain instruction
- CX = CX - 1
- if $Z F=1$ then:
- go back to check_cx
else
- exit from REPE cycle
else
- exit from REPE cycle
example:
open cmpsb.asm from c:\emu8086\examples

Repeat following CMPSB, CMPSW, SCASB, SCASW instructions while ZF $=0$ (result is Not Equal), maximum CX times.

Algorithm:
check_cx:
if $C X$ <> 0 then

- do following chain instruction

| REPNE | chain instruction | - $C X=C X-1$ <br> - if $Z F=0$ then: <br> - go back to check_cx else <br> - exit from REPNE cycle <br> else <br> - exit from REPNE cycle $\square$ |
| :---: | :---: | :---: |
| REPNZ | chain instruction | Repeat following CMPSB, CMPSW, SCASB, SCASW instructions while ZF $=0$ (result is Not Zero), maximum CX times. <br> Algorithm: <br> check_cx: <br> if CX <> 0 then <br> - do following chain instruction <br> - CX = CX - 1 <br> - if ZF $=0$ then: <br> - go back to check_cx else <br> - exit from REPNZ cycle <br> else <br> - exit from REPNZ cycle |
|  |  | Repeat following CMPSB, CMPSW, SCASB, SCASW instructions while ZF = 1 (result is Zero), maximum CX times. <br> Algorithm: <br> check_cx: <br> if $C X$ <> 0 then |


| REPZ | chain instruction | - do following chain instruction <br> - CX = CX - 1 <br> - if $Z F=1$ then: else <br> - go back to check_cx <br> - exit from REPZ cycle <br> else <br> - exit from REPZ cycle |
| :---: | :---: | :---: |
| RET | No operands or even immediate | Return from near procedure. <br> Algorithm: <br> - Pop from stack: <br> - IP <br> - if immediate operand is present: <br> SP = SP + operand <br> Example: <br> ORG 100h ; for COM file. <br> CALL p1 <br> ADD AX, 1 <br> RET ; return to OS. <br> p1 PROC ; procedure declaration. <br> MOV AX, 1234h <br> RET ; return to caller. <br> p1 ENDP |
| RETF | No operands or even immediate | Return from Far procedure. <br> Algorithm: <br> - Pop from stack: <br> - IP <br> - CS <br> - if immediate operand is present: |



Store AH register into low 8 bits of Flags register.
Algorithm:


|  |  | C 0 <br> r r <br> r  <br> OF=0 if first operand keeps original sign. |
| :---: | :---: | :---: |
| SBB | REG, memory memory, REG REG, REG memory, immediate REG, immediate | Subtract with Borrow. <br> Algorithm: <br> operand1 $=$ operand1 - operand2 - CF <br> Example: <br> STC <br> MOV AL, 5 <br> SBB AL, $3 \quad ; A L=5-3-1=1$ <br> RET |
| SCASB | No operands | Compare bytes: AL from ES:[DI]. <br> Algorithm: <br> - AL - ES:[DI] <br> - set flags according to result: OF, SF, ZF, AF, PF, CF <br> - if DF = 0 then - DI = DI + 1 else DI = DI - 1 |
| SCASW | No operands | Compare words: AX from ES:[DI]. <br> Algorithm: <br> - AX - ES:[DI] <br> - set flags according to result: OF, SF, ZF, AF, PF, CF <br> - if $D F=0$ then $\circ D I=D I+2$ |


|  |  | $\begin{aligned} & \text { else } \\ & \qquad \circ \text { DI = DI - } 2 \end{aligned}$ |
| :---: | :---: | :---: |
| SHL | memory, immediate REG, immediate <br> memory, CL <br> REG, CL | Shift operand1 Left. The number of shifts is set by operand2. <br> Algorithm: <br> - Shift all bits left, the bit that goes off is set to CF. <br> - Zero bit is inserted to the right-most position. <br> Example: <br> MOV AL, 11100000b <br> SHL AL, 1 ; $A L=11000000 b, \quad C F=1$. <br> RET <br> OF=0 if first operand keeps original sign. |
| SHR | memory, immediate REG, immediate <br> memory, CL <br> REG, CL | Shift operand1 Right. The number of shifts is set by operand2. <br> Algorithm: <br> - Shift all bits right, the bit that goes off is set to CF. <br> - Zero bit is inserted to the left-most position. <br> Example: <br> MOV AL, 00000111b <br> SHR AL, 1 ; $A L=00000011 b, \quad C F=1$. <br> RET <br> OF=0 if first operand keeps original sign. |


| STC | No operands | Set Carry flag. <br> Algorithm: $C F=1$ $\square$ |
| :---: | :---: | :---: |
| STD | No operands | Set Direction flag. SI and DI will be decremented by chain instructions: CMPSB, CMPSW, LODSB, LODSW, MOVSB, MOVSW, STOSB, STOSW. <br> Algorithm: <br> $D F=1$ $\square$ |
| STI | No operands | Set Interrupt enable flag. This enables hardware interrupts. <br> Algorithm: $\text { IF }=1$ $\square$ |
| STOSB | No operands | Store byte in AL into ES:[DI ]. Update DI. <br> Algorithm: <br> - ES:[DI] = AL <br> - if DF $=0$ then <br> else <br> - DI = DI - 1 <br> Example: <br> ORG 100h <br> LEA DI, a1 |


|  |  | MOV AL, 12h <br> MOV CX, 5 <br> REP STOSB <br> RET <br> a1 DB 5 dup(0) |
| :---: | :---: | :---: |
| STOSW | No operands | Store word in AX into ES:[DI]. Update DI. <br> Algorithm: <br> - ES:[DI] = AX <br> - if $D F=0$ then <br> - DI = DI + 2 <br> else <br> - DI = DI - 2 <br> Example: <br> ORG 100h <br> LEA DI, a1 <br> MOV AX, 1234h <br> MOV CX, 5 <br> REP STOSW <br> RET <br> a1 DW 5 dup(0) <br> unchanged |
| SUB | REG, memory memory, REG REG, REG memory, immediate REG, immediate | Subtract. <br> Algorithm: <br> operand1 = operand1 - operand2 <br> Example: <br> MOV AL, 5 <br> SUB AL, $1 \quad ; A L=4$ <br> RET |


|  |  | $\left\lvert\, \begin{array}{\|c\|c\|c\|\|c\|\|c\|} C \mid & Z & S & 0 & \mid \\ \hline r & \mathrm{~A} & \mathrm{~A} \\ \hline \mathrm{r} & \mathrm{r} & \mathrm{r} & \mathrm{r} \\ \hline \end{array}\right.$ |
| :---: | :---: | :---: |
| TEST | REG, memory <br> memory, REG <br> REG, REG <br> memory, immediate <br> REG, immediate | Logical AND between all bits of two operands for flags only. These flags are effected: ZF, SF, PF. Result is not stored anywhere. <br> These rules apply: $\begin{aligned} & 1 \text { AND } 1=1 \\ & 1 \text { AND } 0=0 \\ & 0 \text { AND } 1=0 \\ & 0 \text { AND } 0=0 \end{aligned}$ <br> Example: <br> MOV AL, 00000101b <br> TEST AL, $1 \quad ; \mathrm{ZF}=0$. <br> TEST AL, 10b ; ZF = 1. <br> RET |
| XCHG | REG, memory memory, REG REG, REG | Exchange values of two operands. <br> Algorithm: <br> operand1 < - > operand2 <br> Example: <br> MOV AL, 5 <br> MOV AH, 2 <br> XCHG AL, AH ; AL = 2, AH = 5 <br> XCHG AL, AH ; AL $=5, A H=2$ <br> RET <br> unchanged |
|  |  | Translate byte from table. Copy value of memory byte at $D S:[B X+$ unsigned AL] to AL register. <br> Algorithm: |


| XLATB | No operands | $A L=D S:[B X+$ unsigned $A L]$ <br> Example: <br> ORG 100h <br> LEA BX, dat <br> MOV AL, 2 <br> XLATB ; $A L=33 h$ <br> RET <br> dat $D B$ 11h, $22 h, 33 h, 44 h, 55 h$ |
| :---: | :---: | :---: |
| XOR | REG, memory <br> memory, REG <br> REG, REG <br> memory, immediate <br> REG, immediate | Logical XOR (Exclusive OR) between all bits of two operands. Result is stored in first operand. <br> These rules apply: <br> 1 XOR $1=0$ <br> 1 XOR $0=1$ <br> 0 XOR $1=1$ <br> 0 XOR $0=0$ <br> Example: <br> MOV AL, 00000111b <br> XOR AL, 00000010b ; AL $=00000101 b$ <br> RET |

